CLAIMS

What is claimed is:

1. A method for adjusting a reference frequency in an electronic device comprising:

determining if a transmission frequency is within a capture range; and

modifying the reference frequency if the transmission frequency is not within the capture range.

2. The method of claim 1 further comprising setting the reference frequency to an initial value.

3. The method of claim 2 wherein the initial value of the reference frequency is a previous reference frequency used by the electronic device.

4. The method of claim 3 wherein the previous reference frequency is a last reference frequency used by the electronic device prior to a last power down of the electronic device.

5. The method of claim 2 wherein the initial value of the reference frequency is a predetermined reference frequency.

6. The method of claim 2 further comprising allowing the reference frequency to stabilize.

7. The method of claim 2 further comprising performing a search of a pilot channel.

8. The method of claim 7 further comprising generating a search result.

9. The method of claim 7 wherein the pilot channel is part of a spread spectrum signal.

10. The method of claim 8 further comprising assigning a code sequence timing to a demodulator using the search result.

11. The method of claim 10 wherein the code sequence timing is a pseudo-noise sequence timing.

12. The method of claim 10 further comprising starting a lock timer.

13. The method of claim 12 wherein, if the demodulator does not lock before the lock timer expires;

modifying the reference frequency;

allowing the reference frequency to become stabilized;

performing another search of the pilot channel; and

generating another search result.

14. The method of claim 13 wherein modifying the clock frequency comprises increasing the clock frequency by an incremental amount.

15. The method of claim 13 wherein modifying the clock frequency comprises decreasing the clock frequency by an incremental amount.

16. The method of claim 12 wherein, if the demodulator does lock before the lock timer expires, enabling automatic frequency control.

17. The method of claim 16 further comprising starting an unlock timer.

18. The method of claim 14 further comprising, if the demodulator does not remain locked when the unlock timer expires:

reassigning the code sequence timing to the demodulator; and

restarting the lock timer.

19. The method of claim 17 further comprising, if the demodulator does remain locked when the lock timer expires, decoding a CDMA signal.

20. A system comprising:

a clock, and

a demodulator coupled to the clock to provide a negative feedback signal to the clock such that a reference frequency generated by the clock is modified.

21. The system of claim 20 wherein the demodulator comprises:

a correlator;

a code sequence generator;

a lock/unlock timer; and

a frequency error detector.

22. The system of claim 21 wherein the code sequence generator is a pseudo-noise sequence generator.

23. The system of claim 21 wherein lock/unlock timer provides the criteria to determine whether to modify a reference frequency generated by the clock.

24. The system of claim 21 wherein the correlator determines an in-phase correlator output and a quadrature-phase correlator output.

25. The system of claim 24 wherein the correlator provides the in-phase correlator output and the quadrature-phase correlator output to the frequency error detector.

26. The system of claim 21 wherein the frequency error detection unit:

determines a frequency error between the clock and a base station; and

generates the negative feedback signal.

27. The system of claim 26 wherein the frequency error detection unit provides the negative feedback signal to the clock.

28. The system of claim 20 further comprising a searcher.

29. The system of claim 28 wherein the searcher;

determines a code sequence timing; and

provides the code sequence timing to the demodulator.

30. The system of claim 29 wherein the code sequence timing is a pseudo-noise sequence timing.

31. The system of claim 20 wherein the clock is a voltage-controlled temperature-compensated crystal oscillator.